

FIG. 1

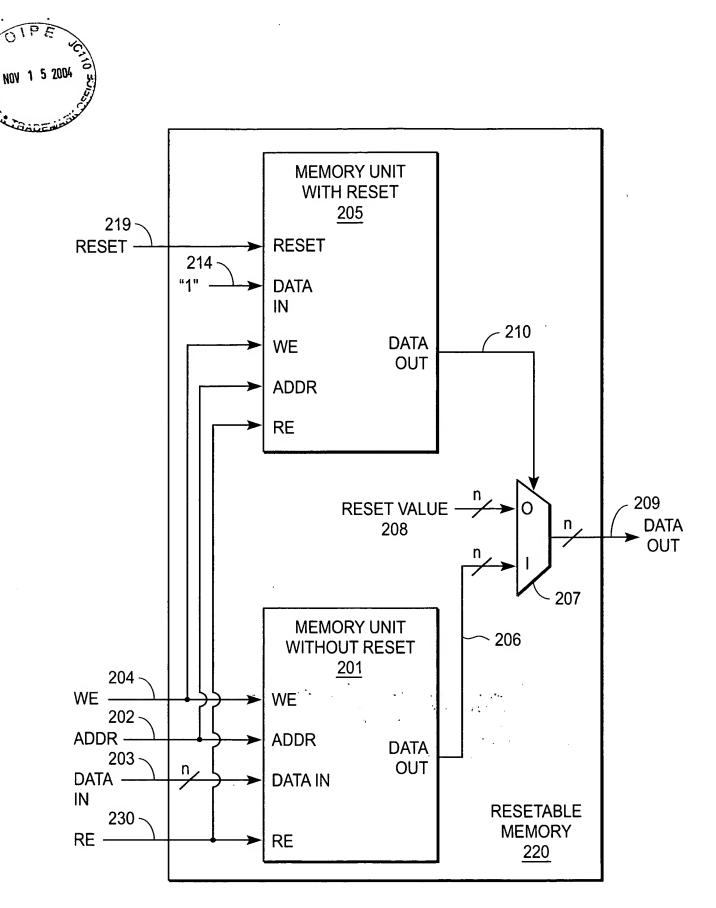


FIG. 2A



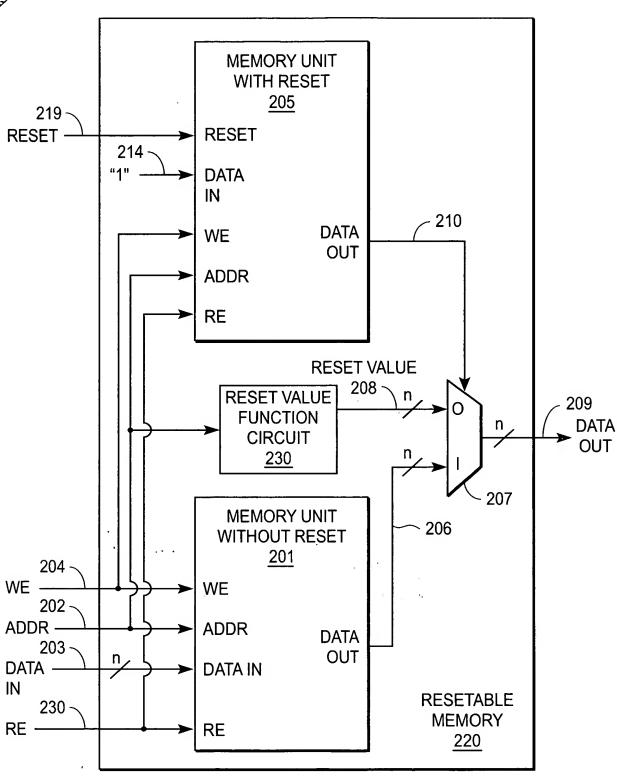


FIG. 2B



```
module synReset(data_in, addr, reset, we, clk, data_out);
parameter data_width = 1024;
parameter addr_width = 10;
parameter RAMsize = 8;
parameter reset_value = 8D0;
input [data_width-1:0] data_in;
input [addr_width-1:0] addr;
input reset, we, clk;
output [data_width-1:0] data_out;
integer i;
reg [data_width-1:0] mem [RAMsize-1:0];
wire [data_width-1:0] data_out;
//synthesis loop_limit 2000
always @(posedge clk)
begin
       if(reset == 1b1)
       begin
              for (i=0; i < RAMsize; i=i+1)
                     begin
                            mem[i] = reset_value;
                     end
       end else if(we == 1b1)
       begin
                     mem[addr] = data_in;
       end
end
assign data_out = mem[addr];
endmodule
```



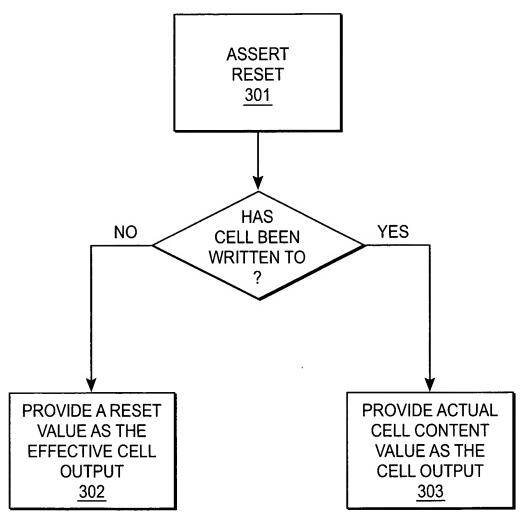


FIG. 3



INFER EXISTENCE OF MEMORY
WITH RESET FROM BEHAVIORAL
LEVEL CIRCUIT DESCRIPTION
OR RTL LEVEL CIRCUIT
DESCRIPTION
401

INCORPORATE RESETABLE
MEMORY INTO CIRCUIT
DESCRIPTION
402

## FIG. 4



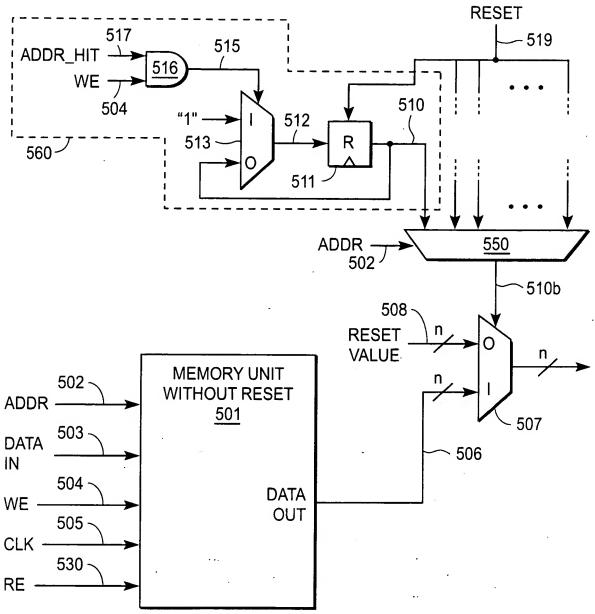


FIG. 5



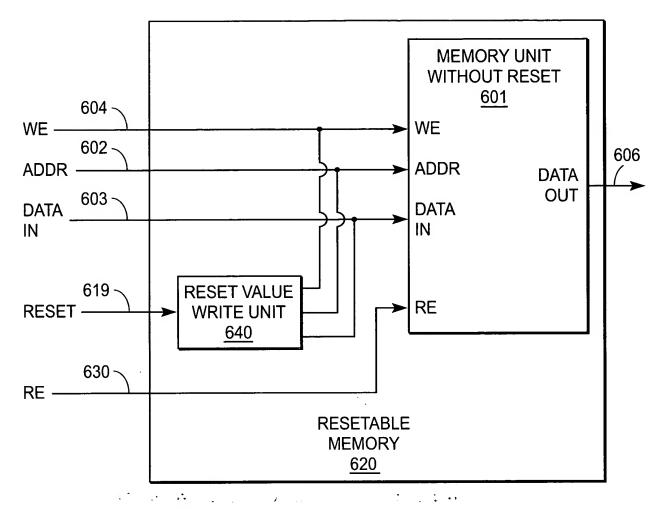


FIG. 6



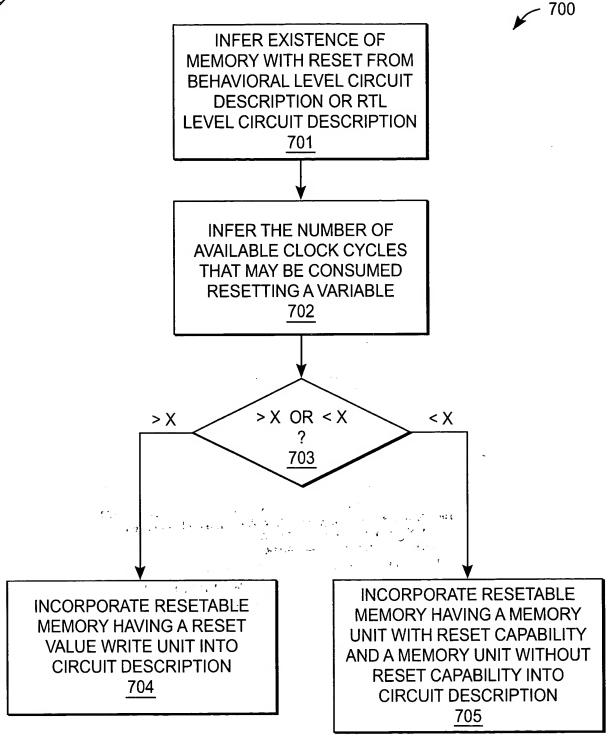


FIG. 7



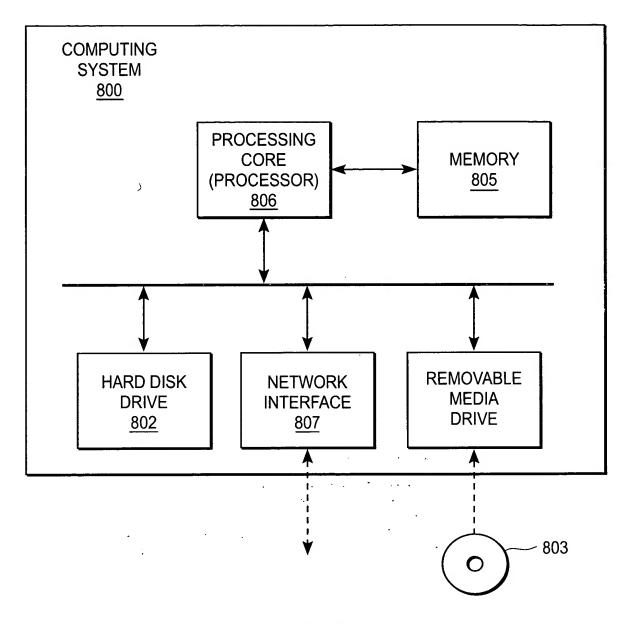


FIG. 8